ANALOG DEVICES

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APPLICATION NOTE

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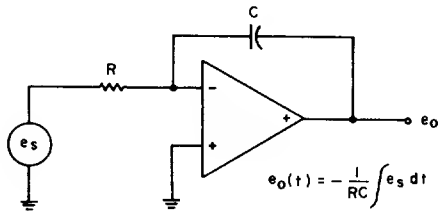
Operational Integrators

by Ray Stata

Modern solid state operational amplifiers make remarkably good integrators. Almost any degree of accuracy can be achieved depending on the choice of the amplifier and the feedback capacitor. A great deal of literature exists† which discusses integrator error in analog computers and this subject will not be covered here. But we shall review the non-ideal characteristics of operational amplifiers (and to some extent capacitors) which limit the performance of integrators in instrumentation circuits. This we hope will help the reader make a better choice of amplifiers for his particular application.

†Korn and Korn, *Electronic Analog and Hybrid Computers* — McGraw Hill.

An ideal operational amplifier for integrator applications would have infinite open loop gain and input impedance and zero offset voltage and current (that is, $e_o = o$, when $e_s = o$). For this case, Figure 1 shows the characteristics of an ideal integrator.



$$\frac{e_o(s)}{e_s(s)} = \left(-\frac{1}{RC}\right)\left(\frac{1}{S}\right) \frac{\text{VOLTS/SEC}}{\text{VOLT}}$$

Figure 1. Ideal Operational Integrator

The gain (or characteristics time) of the circuit is given by 1/RC, which is to say that the output will change by (1/RC) volts/sec for each volt of input signal. The input impedance as viewed from the source voltage, e_s, is determined by the value for R.

OFFSET AND DRIFT ERRORS

By far the greatest source of error in integrators is due to offset and drift of the amplifier. An equivalent circuit is given in Figure 2 from which we can predict the errors due to offset. For the moment we shall assume that open loop gain, A, and open loop input impedance, R_d, are infinite.

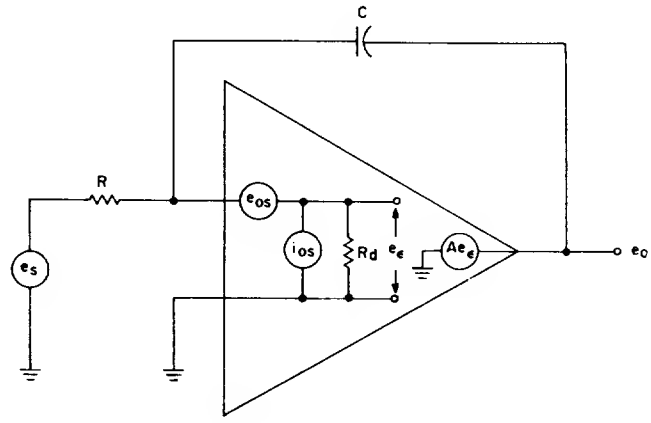


Figure 2. Equivalent Circuit for Integrator

$$e_{os} = \underset{\substack{\mu V \\ \text{at} \\ 25°C}}{E_{os}} + \underbrace{\frac{\Delta e_{os}}{\Delta T}}_{\mu V/°C}\Delta T + \underbrace{\frac{\Delta e_{os}}{\Delta V_s}}_{\mu V/\%}\Delta V_s + \underbrace{\frac{\Delta e_{os}}{\Delta t}}_{\mu V/day}\Delta t$$

$$i_{os} = \underset{\substack{\text{pa} \\ \text{at} \\ 25°C}}{I_{os}} + \underbrace{\frac{\Delta i_{os}}{\Delta T}}_{\text{pa}/°C}\Delta T + \underbrace{\frac{\Delta i_{os}}{\Delta V_s}}_{\text{pa}/\%}\Delta V_s + \underbrace{\frac{\Delta i_{os}}{\Delta t}}_{\text{pa/day}}\Delta t$$

As shown the offset voltage, e_{os}, and the offset current, i_{os}, can be calculated for any temperature, supply voltage and time period from the drift coefficients of the amplifier. It is usually possible to adjust the initial offset voltage and current, E_{os} and I_{os}, to zero by some biasing network.

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The simplest way to analyze offset errors is to refer them to the source voltage as shown in Figure 3. In this case offset current is multiplied by R and becomes a voltage source. When viewed at the

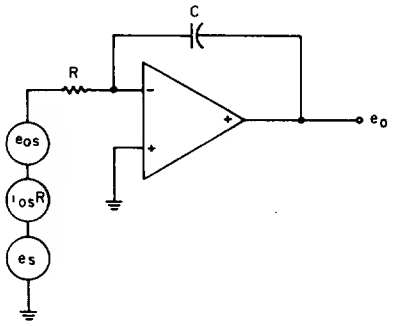

Figure 3. Offsets Referred to the Input

input, the offsets cannot be distinguished from the input signal and hence introduce a basic error in the integration of the signal. The percentage error would be, % error $= (e_{os} + i_{os}R)\ 100/\bar{e}_s$, where $\bar{e}_s$ is the time average of the input signal over the integration period. Notice that R should be as small as possible to minimize offset errors for a given amplifier. But remember that R also sets the input impedance for the integrator.

When referred to the input, the analysis of offset errors is not much different for an integrator than for an inverting DC amplifier. More detailed information is given on this subject in an Analog Devices' application note entitled "Part IV, Offset and Drift in Operational Amplifiers."

In some applications it is necessary to refer the offset error to the output in order to derive meaningful results. In this case the output error is a drift rate which is given by,

$$\frac{de_o}{dt} = \frac{e_{os} + Ri_{os}}{RC} = \frac{e_{os}}{RC} + \frac{i_{os}}{C}$$

Again, we see that output drift rate is minimized by using the smallest value for R and the largest value for C. This follows since the drift rate due to offset voltage is fixed by the gain of the circuit (1/RC) whereas the drift rate due to offset current is reduced by using a larger C.
The practical limits on the choice of R and C are as follows:

1. Source impedance sets a minimum value on input impedance which is equal to R.
2. The physical size, price and quality are all serious problems in using large value capacitors particularly when greater than 1 to 5μf.

For differential input amplifiers, the error due to offset current is generally reduced by balancing the impedance as seen from each input to ground. For the circuit in Figure 3 this would amount to inserting a resistor from the plus input to ground equal to R. Due to the input symmetry of a differential amplifier, offset current at each input tends to be equal and tends to track with temperature and thus the drift error is reduced by balancing impedances.

ERRORS DUE TO FINITE GAIN, INPUT IMPEDANCE AND BANDWIDTH

The open loop gain response for most operational amplifiers can be represented by the graph in Figure

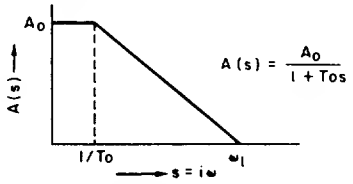

Figure 4. Typical Open Loop Gain Response

4. If we go back to Figure 2 and assume that the amplifier has to gain response of Figure 4 and an open loop input impedance, R_d, then the exact expression for integrator gain would be:

$$\frac{e_o(s)}{e_s(s)} = \underbrace{\left[\frac{-1}{RCs}\right]}_{\text{ideal}} \underbrace{\left[\frac{1}{1 + \left(\frac{1 + T_o s}{A_o}\right)\left(1 + \frac{1}{R_p C s}\right)}\right]}_{\text{error due to finite gain and bandwidth}} \quad (1)$$

where $R_p = R_d R / R_d + R$ (parallel sum)

Equation (1) can be simplified if we assume that $A_o >> 1$ (a very safe bet):

$$\frac{e_o(s)}{e_s(s)} = \left[\frac{-1}{RCs}\right]\left[\frac{1}{1 + \frac{s}{\omega_1} + \frac{1}{A_o R_p C s}}\right] \text{ for } A_o >> 1 \quad (2)$$

where $\omega_1 \approx A_o/T_o$ is the amplifier unity gain bandwidth.

HIGH FREQUENCY ERRORS DUE TO FINITE BANDWIDTH

Finite amplifier bandwidth imposes some limitation on the ability of the integrator to respond to instantaneous input changes. The transient behavior at $t = o$ can be predicted by examining the behavior of equation (2) at high frequencies. In this case equation (2) becomes:

$$\frac{e_o(s)}{e_s(s)} = \frac{-1}{RCs}\left(\frac{1}{1 + s/\omega_1}\right) \text{ for } s >> \frac{1}{A_o R_p C} \quad (3)$$

This is the equation for an ideal integrator except for a time lag which is inversely proportional to the unity gain bandwidth, ω_1. To illustrate the error due to finite bandwidth, consider the response of (3) to a step function input as given by (4) and Figure 5.

$$e_o(t) \approx \frac{1}{RC}\left(t - 1/\omega_1\right) \text{ for } e_s(t) = -\mu_{-1}(t) \quad (4)$$

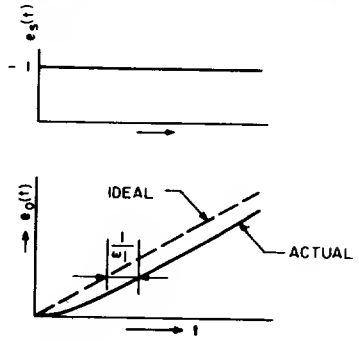

Figure 5. Step Response of Integrator at t = o

Note that the time lag depends only on amplifier open loop bandwidth, ω_1, and is independent of the values for R and C.

LOW FREQUENCY ERRORS DUE TO FINITE GAIN

The behavior of an integrator over long time periods can be predicted by the low frequency response of the circuit. In this case, where $s << \omega_1$, equation (2) becomes:

$$\frac{e_o(s)}{e_s(s)} = \left[\frac{-1}{RCs}\right]\left[\frac{1}{1+\frac{1}{A_oR_pCs}}\right] = -\frac{A_oR_p/R}{1+A_oR_pCs} \qquad (5)$$

Insight is gained into the operation of integrators at low frequencies by realizing that (5) is equivalent to the response of an ideal integrator with an infinite gain and input impedance amplifier, but with a feedback resistor A_oR_p in parallel with the feedback capacitor as shown in Figure 6.

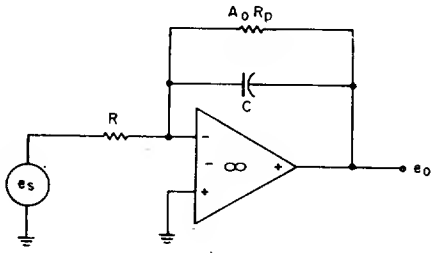

Figure 6. Integrator Low Frequency Equivalent Circuit

To illustrate more clearly the effect of low frequency errors, consider the response of (5) to a step function input as given by (6) and Figure 7.

$$e_o(t) = \frac{R_pA_o}{R}(1-e^{-t/A_oR_pC}), \text{ for } e_s(t) = -\mu_{-1}(t) \qquad (6)$$

Expanding (6) into a power series we have:

$$e_o(t) = \frac{t}{RC} - \frac{t^2}{2A_o(R_pC)\,(RC)} + - - -$$

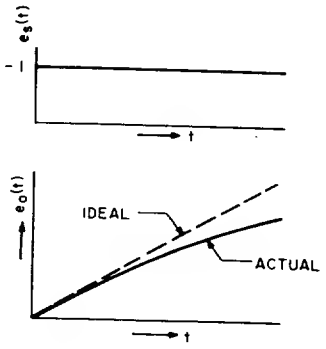

Figure 7. Step Response Showing Low Frequency Error Due to Finite Gain

The first term in this series is the response for an ideal integrator, while the second term is the principle error component which grows as the square of time.

In summary low frequency integrator errors are inversely proportional to finite open loop voltage gain. This follows from the fact that with finite gain the error voltage is not zero, as usually assumed, which tends to reduce input current as the output grows.

INTEGRATOR HOLD ERRORS

One important use of integrator circuits is to precisely remember or hold a voltage potential. Finite amplifier gain causes a fixed integrator output voltage to droop.

Intuitively it is apparent from Figure 6 that the effective leakage resistance, A_oR_p, due to finite voltage gain and input impedance tends to discharge any fixed voltage stored across the feedback capacitor.

To develop a quantitative expression for this error, assume that the circuit in Figure 6 has the initial condition $e(o) = E_o$ and that $e_s = o$. In this case, the output voltage is simply:

$$e_o(t) = E_oe^{-t/A_oR_pC}$$

By expansion this becomes:

$$e_o(t) = E_o - E_o\left[\frac{t}{A_oR_pC} - \frac{t^2}{2(A_oR_pC)^2} + - - -\right] \qquad (7)$$

The first item of (7) is the output of an ideal integrator, while the terms in the brackets represent the errors due to finite gain. Figure 8 shows integrator hold error.

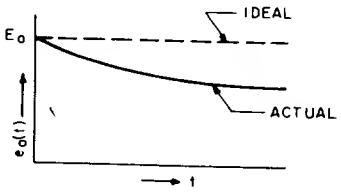

Figure 8. Integrator Hold Error

It is interesting to note that minimum error is obtained in hold operation when the input resistor is open circuited rather than short circuited. In this case the equivalent circuit is shown in Figure 9.

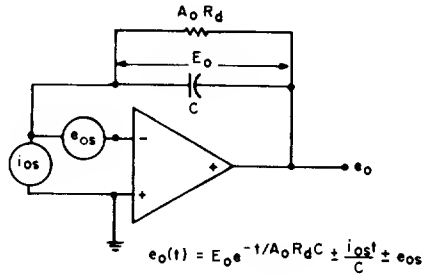

Figure 9. Hold Circuit with Input Open

Note that the equivalent feedback leakage resistor is determined only by the open loop input impedance and gain (A_oR_d). Further, the output drift rate is determined only by the offset current. Voltage offset appears at the output as a fixed offset.

FEEDBACK CAPACITOR

The performance of operational amplifiers have now reached the point where the quality of the feedback capacitor can limit the accuracy in the most precise applications. Therefore a brief discussion of capacitor limitations will be helpful in precise integrator design.

The chart in Figure 10 shows the salient characteristics for various types of high quality capacitors. This data was compiled with the assistance of Southern Electronics Corporation, Burbank, California, a capacitor manufacture who specializes in high quality capacitors for integrator applications. An application note from this company entitled "Capacitor Talk" gives more information on the interpretation of capacitor specifications.

In analog computers where scale factor accuracy is important it is common practice to enclose the feedback capacitor in a temperature controlled oven. In this case long term stability of capacitance value for polystyrene and mylar capacitors is about 0.1% per year.

Insulation Resistance — One important limitation for integrator capacitors is insulation or leakage resistance. The specification used to define this limitation usually is expressed in megohms - microfarads, which is equivalent to the time in seconds for a fixed voltage stored on the capacitor to discharge to 63% of its initial value. As a general rule the maximum insulation resistance is about two times the value for a one microfarad capacitor, which establishes the limit for insulation resistance of small capacitor values.

Dielectric	Mylar	Metalized Mylar	Poly-carbonate	Metalized Poly-carbonate	Polystyrene	Teflon	Metalized Teflon
Temperature Range							
Hi Temp (°C)	+125	+125	+125	+125	+85	+200	+200
Lo Temp (°C)	−65	−65	−65	−65	−65	−65	−65
Temperature Coefficient							
−65°C to 25°C (%)	−6	−6	−1.5	−1.5	+0.9	+1.9	+0.5
25°C to Hi Temp (%)	+12	+12	±0.5	±0.5	−0.6	−3.7	−1.0
Dielectric Absorption							
% @ 25°C	0.1	0.1	.05	.05	.02	.01	.02
Dissipation Factor							
@25°C (%)	0.3	0.5	0.1	0.2	0.02	0.01	0.1
@ Hi Temp (%)	1.2	1.7	0.07	0.6	0.04	0.02	0.2
Insulation Resistance							
@ 25°C (MΩ-μf)	$2x10^5$	$5x10^4$	$4x10^5$	$2x10^5$	$1x10^6$	$1x10^6$	$5x10^5$
@ Hi Temp (MΩ-μf)	$3x10^2$	$1x10^2$	$1.5x10^4$	$15x10^2$	$7x10^4$	$1x10^5$	$2.5x10^4$
Approximate Size for 50Vdc							
cubic inch/μf (uncased)	.12	0.06	.19	0.09	.44	1.1	0.39

Figure 10. Comparison of Capacitor Specifications

The effect of insulation resistance can be represented in Figures 6 and 9 as another resistance in parallel with A_oR_p or A_oR_d and the issuing equations are modified accordingly. The insulation resistance of the very best capacitors is about 10^{12} ohms. By comparison a chopper stabilized operational amplifier will have open loop input impedance, R_d, of 10^6 ohms and open loop gain, A_o, of 10^8 giving an equivalent resistance of 10^{14}. Even an inexpensive differential amplifier will have equivalent leakage resistance of 10^{10} to 10^{11} ohms. Thus we see that the capacitor and not the amplifier usually sets the limit on performance in this regard.

Dielectric Absorption — One of the single most important dynamic errors of integration is due to dielectric absorption. This error results from the fact that when a capacitor is charged or discharged not all of the dielectric polarization takes place immediately. Consequently there can be an appreciable residual voltage with a relatively long time constant. The specification given for this parameter is the residual voltage expressed as a percentage of the applied voltage measured approximately one second after the capacitor is discharged. Polystyrene and teflon are mostly used for precision integrators since these materials have small but measurable errors due to dielectric absorption. For additional information on analyzing this source of error you should refer to "An Analysis of Certain Errors in Electronic Differential Analyzers II—Capacitor Dielectric Absorption," P. C. Dow, IRE Trans. on Electronic Computers, Vol. EC-7, pp.17-22, March, 1958.

Dissipation Factor, which is related to dielectric absorption, can be termed the sum total of all the losses in the capacitor and is expressed as the percentage ratio of the effective series resistance to the reactive capacitance, or as the tangent of the loss angle. Dissipation factor is important in AC integrators or in analog computers where repetitive integration is performed.

LEAKAGE RESISTANCE

In the highest performance integrators, leakage resistance to the summing junction or across the feedback capacitor can play a large role in the attainable performance. It is extremely important to shield the summing junction and its leads from leakage paths to potentials other than ground. For example, offset current, which is one of the principle limitations to good integrator performance, in a good chopper amplifier is about 10^{-11} amps. The insulation resistance required to keep the leakage current from the 15VDC supply voltage less than 10^{-11} amp would have to be greater than one million megohms. The insulation resistance of most wire and connectors fall short of this requirement. However, by properly shielding the summing junction and its leads, leakage currents from active sources are shunted to ground, effectively creating extremely high insulation resistance from these potentials to the summing junction.

By the same token leakage resistance of the clamping circuits across the feedback capacitor used to reset the integrator should not be overlooked when calculating the effective leakage of a feedback capacitor. For example, the leakage resistance of a computer grade capacitor is typically 10^{12} ohms, which may be negligible compared to the leakage resistance of a relay or a solid state switch.

AC INTEGRATORS

In some applications it may be desirable to integrate AC signals over a reasonably long time and it may not be possible to reset the output to zero periodically. In this case the DC offset problem can be alleviated in part by bounding the DC closed loop gain as shown in Figure 11.

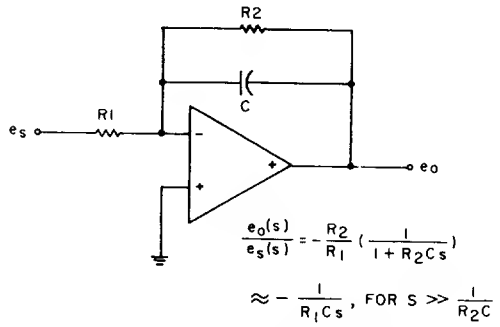

Figure 11. AC Integrator

The closed loop response for this circuit is shown in Figure 12.

For frequencies greater than $1/R_2C$ the response approaches that of an ideal integrator with gain of $1/R_1C$. For example, for signal frequencies, ω_s, a decade away from the corner frequency, $1/R_2C$, the gain error is only .5%.

The advantage of bounding the DC gain with R_2 is that the amplifier output will not drift into saturation. Instead the output will assume a DC value of $e_o = -R_2/R_1\,(e_{os} + R_1 i_{os})$. This output will limit the dynamic range for AC output signals; but, by choosing an amplifier with sufficiently low offsets, satisfactory operation can be obtained for many AC integrator applications.

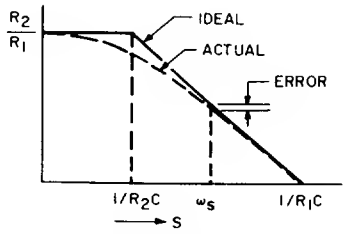

Figure 12. Gain Response for AC Integrator

For integration of very low frequency AC signals, the DC gain requirements of the previous circuit are so large as to cause saturation of the output. In this case the following circuit allows the DC gain to be reduced.

The lowest frequency which can be accurately integrated is limited by the size for C_2. The general expression for the corner frequencies ω_1 and ω_2 are rather complex and as a practical matter can only be determined by trial and error calculations. The lowest signal frequency, ω_s, should be at least ten times greater than ω_2.

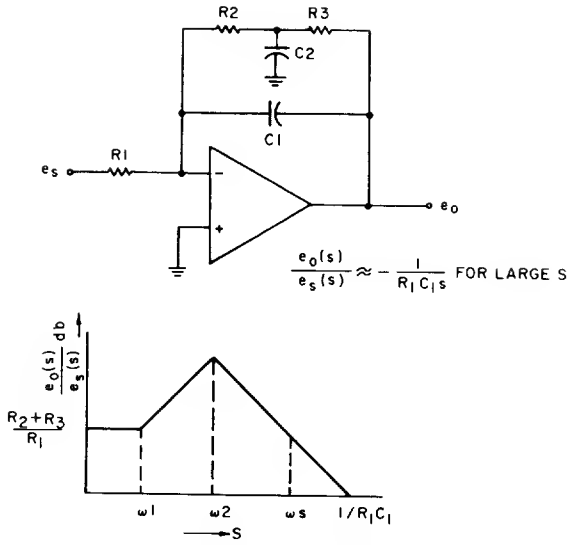

Figure 13. Low Frequency AC Integrator